

Application No. 10/595,658

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of:

Applicant: Adam CAPEWELL et al.

Application No: 10/595,658

Filing Date: May 3, 2006

Title: FORMATION OF LATTICE-TUNING SEMICONDUCTOR SUBSTRATES

REQUEST FOR CORRECTED FILING RECEIPT

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Respectfully submitted,

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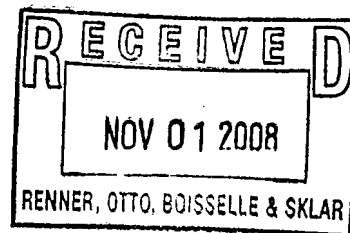
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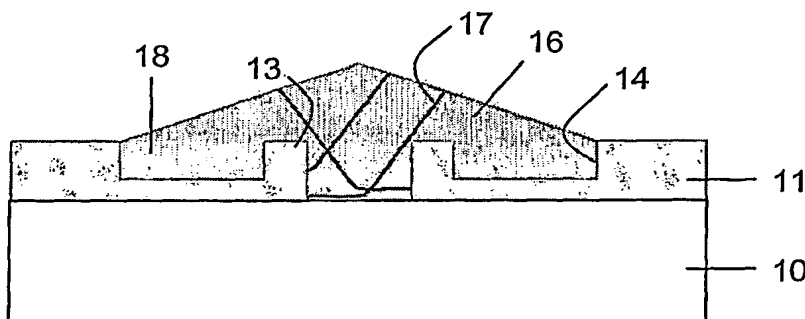
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(54) Title: FORMATION OF LATTICE-TUNING SEMICONDUCTOR SUBSTRATES



(57) Abstract: A method of forming a
lattice-tuning semiconductor substrate
comprises defining a selected area
(12) of a Si surface (15) by means of
a window (13) extending through an
isolating layer (11) on the Si surface
(15); defining in the isolating layer (11)
a depression (14) separated from the Si
surface (15) by a portion of the isolating
layer (11); growing a SiGe layer (16)
on top of the selected area (12) of the Si
surface (15) such that dislocations (17)
are formed in the window (13) to relieve
the strain in the SiGe layer (16); and

further growing the SiGe layer (16) to overgrow the isolating layer (11) and extend into the depression (14) to form a substantially dislocation-free area (18) of SiGe within the depression (14). If required, the portion of the SiGe layer (16) that has overgrown the isolating layer (11) can then be removed by polishing so as to isolate the substantially dislocation-free area (18) of SiGe within the depression (14) from the area of SiGe within the window (13). Furthermore the SiGe layer (16) and the isolating layer (11) can then be removed from the Si surface (15) except in the vicinity of the depression (14) so as to leave on the Si surface (15) the substantially dislocation-free area (18) of SiGe isolated from the Si surface (15) by the portion of the isolating layer (11).

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